AMENDMENTS TO THE CLAIMS

1. (Canceled) A logic cluster in logic block of a field programmable gate array, comprising:

a first look-up table (LUT) having a plurality of inputs and a single output;

a second LUT having a plurality of inputs and a single output;

a D-type flip-flop having an input and an output;

a first n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a first signal and said source connected to said output of said first LUT;

a second n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a second signal, said source connected to said output of said second LUT and said drain connected to said drain of said first n-channel MOS pass transistor to form a node connected to said input of said D-type flip-flop;

a third n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said first signal and said source connected to said output of said first LUT;

a fourth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said second signal and said source connected to said output of said second LUT;

a fifth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to said first signal and said source connected to said drain of said third n-channel MOS pass transistor;

a first inverter having an input and an output, said input connected to said drain of said third n-channel MOS pass transistor;

a second inverter having an input and an output, said input connected to said drain of said fifth n-channel MOS pass transistor;

a seventh n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a third signal and said source connected to said output of said first inverter;

an eighth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said third signal, said source connected to said output of said second inverter and said drain connected to said drain of said seventh n-channel MOS pass transistor to form a node as a first output of said logic cluster;

a ninth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a fourth signal and said source connected to said output of said second inverter; and

a tenth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said fourth signal, said source connected to said output of said first inverter and said drain connected to said drain of said ninth n-channel MOS pass transistor to form a node as a second output of said logic cluster.

2. (New) A logic cluster in a logic block of a field programmable gate array, comprising:

a plurality of look-up tables wherein each of said plurality of look-up tables has a plurality of inputs and a single output;

a D-type flip-flop having an input and an output;

a first plurality of NMOS transistors wherein a source of each of said first plurality is connected to an output of different ones of said plurality of look-up tables and said drain is connected to an input of said D-type flip-flop and a gate controlled by a first signal;

a second plurality of NMOS transistors wherein a source of each of said first plurality is connected to an output of different ones of said plurality of look-up tables and said drain is connected to an output of said D-type flip-flop and a gate controlled by a complement of said first signal controlling said gate of the one of said first plurality of NMOS transistors having a source connected to said output of different one of said plurality of look-up tables;

a third plurality of NMOS transistors wherein each of said third plurality of NMOS transistors has a source connected said drain of one of said second plurality of NMOS transistors, a gate connected to said output of said D-type output device and gates of other ones of said third plurality of transistors, and a gate controlled by said first signal controlling said one of said first plurality of NMOS transistors connected to said ones of said second plurality of transistors connected to said source;

a plurality of inverters wherein each of said inverters is connected to a drain of one of said second plurality of transistors and said source of said one of said third plurality of transistors connected to said drain of said one of second plurality of transistors;

a fourth plurality of NMOS transistors wherein each of said plurality of fourth NMOS transistors has a source connected to one of said plurality of invertors, a drain connected to one of a plurality of output nodes, and a gate controlled by a second signal; and

a fifth plurality of NMOS transistors wherein each of said plurality of fifth NMOS transistors has a source connected to one of said plurality of invertors, a drain

connected to one of a plurality of output nodes wherein said one of said plurality of output nodes is connected to a drain of one of said fourth plurality of NMOS transistors connected to another one of said plurality of transistors, and a gate controlled by an inverse of said second signal controlling said one of said fourth plurality of NMOS transistors.